Company	Trenz Electronic GmbH
PCN Number	PCN-20240621a
Title	TE0821-01 to TE0821-02 Hardware Revision Change (Revised)
Subject	Hardware Revision Change
Issue Date	(2024-07-22), Revised 2024-10-08

Products Affected

This change affects all Trenz Electronic TE0821 SoMs: TE0821-01*.

Affected Product	Changes	Replacement
TE0821-01-3BE21MA	#1, #3 ... #32	TE0821-02-3BE81MA
TE0821-01-3BE21MC	#1, #3 ... #32	TE0821-02-3BE81MC
TE0821-01-3BE21ML	#1, #3 ... #32	TE0821-02-3BE81ML
TE0821-01-3BI21MA	#1, #3 ... #32	TE0821-02-3BI81MA
TE0821-01-4DE31ML	#2 ... #32	TE0821-02-4DE91ML
TE0821-01-2AE31PA	#2 ... #32	TE0821-02-2AE91PA
TE0821-01-3AE31PA	#2 ... #32	TE0821-02-3AE91PA
TE0821-01-3BI91ND	#3 ... #32	TE0821-02-3BI91ND

Changes

#1 Changed DDR4 SDRAM (U2, U3) from K4A8G165WB-BIRC to K4A8G165WC-BITDTCV.

Type: BOM change

Reason: BOM Optimization.

Impact: DDR timing needs to be considered in customer design. Trenz Reference Design reflects it without changing timing but custom firmware needs to be checked and eventually updated by customer.

#2 Changed DDR4 SDRAM (U2, U3) from K4AAG165WB-MCRC0CV to MT40A1G16TB-062E IT:F, set termination resistor (R94) from fitted to not fitted, and changed resistor (R68, R69) from 240 Ohm to 0 Ohm.

Type: BOM change

Reason: BOM Optimization.

Impact: DDR timing needs to be considered in customer design. Trenz Reference Design reflects it but custom firmware needs to be checked and probably updated by customer.

#3 Changed reset, enable and power-up structure with added resistor (R113 ... R115) (Default R113: not fitted) and added transistor T2.

Type: Schematic Change

Reason: Improve module reset, enable, and power-up.

Impact: Module reset, enable, and power-up handling is modified. Two different options are possible: (1) Standard option: Signal "EN" only enables DCDC U5 and DCDC U12 and CPLD U21 pin 27 is connected to signal "POR_B" via voltage translator T2; (2) Backwards compatible option: "EN" signal from B2B connector enables DCDC U5 **and** DCDC U12 **and** can be monitored by CPLD U21 pin 27; Therefore, please, verify that the module meets your requierements.

#4 Changed power sequencing according to power diagram.

Type: Schematic Change

Reason: Follow (more closely) AMD recommended power sequence.

Impact: Sequence of external (B2B) available power rails is not changed. A slightly enlarged time constant between "EN" high and power up of 1.8V rail could be observed.

#4.1 Enable DCDC (U12) via net "EN".

Type: Schematic Change

Reason: Refer to #4.

Impact: Refer to #4.

#4.2 Enable DCDC (U27) via net "PG_0V85".

Type: Schematic Change

Reason: Refer to #4.

Impact: Refer to #4.

#4.3 Changed DCDC (U20) power-up from net "PG_0V85" to "PG_PSLP_INTIO". DCDC (U27) enables DCDC (U20).

Type: Schematic Change

Reason: Refer to #4.

Impact: Refer to #4.

#4.4 Changed power sequence: DCDC (U26) enables DCDC (U4, U23) via net "PG_FP0V85".

Type: Schematic Change

Reason: Refer to #4.

Impact: Refer to #4.

#4.5 Changed power sequence: DCDC (U4) enables DCDC (U9) via net "PG_DDR2V5".

Type: Schematic Change

Reason: Refer to #4.

Impact: Refer to #4.

#4.6 Changed resistor (R70) functionality from pull-up resistor for DCDC (U9) to pull-up resistor for DCDC (U26).

Type: Schematic Change

Reason: Refer to #4.

Impact: Refer to #4.

#4.7 Added pull-up resistor (R122).

Type: Schematic Change

Reason: Refer to #4.

Impact: Refer to #4.

#5 Changed DCDC (U5) from EN6363QI to MPM3860GQW-Z.

Type: Schematic Change

Reason: EOL of Component.

Impact: None. Minor changes in electrical characteristics.

#6 Changed load switch TPS27081ADDCR (Q1) to MP5077GG-Z and adapted circuit.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None. Increased current output capability. Minor changes in electrical characteristics.

#7 Changed monitored power supply rail for voltage monitor TPS3106K33DBVR (U19) from "PS_LP0V85" to "PS_FP0V85".

Type: Schematic Change

Reason: Follow AMD recommendation.

Impact: None. Release of signal "POR_B" is done after power supply rail "PS_FP0V85" is higher than threshold of voltage monitor.

#8 Added optional voltage detector BD39040MUF-CE2 (U28) and connected it to system controller (U21) pin 5 via net "PG_ALL" which is pulled-up to power rail "3.3VIN" with resistor (R102).

Type: Schematic Change

Reason: Improve power monitoring.

Impact: Improved power monitoring circuit by supervising additional voltage rails. If monitored voltages are out of range signal "PG_ALL" is deasserted.

#9 Removed pull-up resistor (R82) from signal "MR".

Type: Schematic Change

Reason: Use internal pull-up resistor.

Impact: None.

#10 Added capacitor (C143) for signal "MR".

Type: Schematic Change

Reason: Improve noise immunity.

Impact: None.

#11 Added diode (D5) between U19 pin 3 net "MR" and voltage rail "3.3V".

Type: Schematic Change

Reason: Protect manual reset pin.

Impact: None.

#12 Enabled DDR4 test usage via connecting signal "DDR4-TEN" together for DDR4 memory (U2, U3) and pulling them down via 499 Ohm resistor (R100). Added testpoint (TP17) for signal "DDR4-TEN".

Type: Schematic Change

Reason: Enable DDR4 test improvement.

Impact: None.

#13 Connected unused SoC (U1) bank 64 IO pins and VCCO pins together to net "GND".

Type: Schematic Change

Reason: Improvement ESD protection.

Impact: None.

#14 Improved voltage rail VTT layout and added decoupling capacitor (C179 ... C185).

Type: Schematic Change

Reason: VTT layout and decoupling improvement.

Impact: Improved VTT voltage rail reliabililty.

#15 Added pull-up resistor (R116) (Default: not fitted) and pull-down resistor (R117) to add pull-up/-down option for SoC "POR_OVERRIDE" signal.

Type: Schematic Change

Reason: Add feature to allow assembly options with POR Override "high".

Impact: None. Assembly option with power override possible.

#16 Added pull-up resistor for "HOLD"-function (R118, R120) and "WP"-function (R119, R121) for flash (U7, U17).

Type: Schematic Change

Reason: Improved SPI interface usage with different flashs.

Impact: None.

#17 Added additional decoupling capacitor (C144, C178, C186 ... C189).

Type: Schematic Change

Reason: Improve power supply decoupling.

Impact: None.

#18 Changed 220 nF capacitor (C61) from 16 V, X7R, 0402 to 6.3 V, X5R, 0201.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

#19 Changed capacitor (C12 ... C16, C45, C49, C52, C53, C57) from 4.7 µF, 6.3 V, to 10 µF, 10 V.

Type: Schematic Change

Reason: AMD recommendation.

Impact: None.

#20 Changed 10 µF capacitor (C2, C18, C20, C22, C37, C41, C48, C82, C89, C92, C94, C95, C107, C130, C132, C134) from 16 V, 0603 to 10 V, 0402.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

#21 Changed 22 µF capacitor (C19, C21, C23, C67, C84, C93, C129, C133, C135) from 6.3 V to 10 V.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

#22 Changed capacitor (C136, C140) from 22 µF to 47 µF.

Type: Schematic Change

Reason: AMD recommendation.

Impact: None.

#23 Changed 47 µF capacitor (C24, C25, C27, C33, C34, C88, C96, C110) from 0805 to 0603.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

#24 Changed ferrid bead (L1... L3, L5, L7, L9 ... L12) from BKP0603HS121-T to MPZ0603S121HT000.

Type: BOM Change

Reason: EOL of component.

Impact: None.

#25 Changed 10 kOhm resistor (R36, R51, R87) from 50 mW, 0201 to 63 mW, 0402.

Type: BOM Change

Reason: BOM Optimization.

Impact: None.

#26 Changed net names "PG_PS_LP" to "PG_PSLP_INTIO", "PS_AVCC" to "PS_MGTRAVCC", "PG_AVCC" to "PG_MGTRAVCC", "OTG_RCLK" to "OTG_REFCLK", "PS_AVTT" to "PS_MGTRAVTT", and "PG_DDR" to "PG_DDR1V2".

Type: Schematic Change

Reason: Documentation Improvement

Impact: None.

#27 Added testpoints (TP18, TP21 ... TP25).

Type: Schematic Change

Reason: Voltage and system monitoring improvement.

Impact: None.

#28 Changed signal trace lengths.

Type: PCB Change

Reason: Result of changes above.

Impact: Changed trace length have to be taken into account in existing designs. The trace length for new revision will be available in TE0821 series pinout generator[1]. Please check if change in trace length still matches your requirements. Adaption of carrier may be necessary.

#29 Updated "FPGA Speed grade" information table on page "TE0821 - POWER".

Type: Documentation Update

Reason: Documentation Improvement

Impact: None.

#30 Added power diagram. Updated system overview and revision history. Updated page count and order.

Type: Documentation Update

Reason: Documentation Improvement.

Impact: None.

Following changes are added in revised PCN version:

#31 Changed clock (U11) from SiT8008BI-73-XXS-25.000000E to SIT8008BI-73-18S-25.000000E.

Type: BOM change

Reason: Follow Ethernet PHY recommendation.

1 https://shop.trenz-electronic.de/trenzdownloads/Trenz_Electronic/Pinout/4x5_series_pinout_tracelength.xlsx

Impact: None.

#32 Adapted power supply for clock (U11) and clock generator (U10) from 3.3 V to 1.8 V.

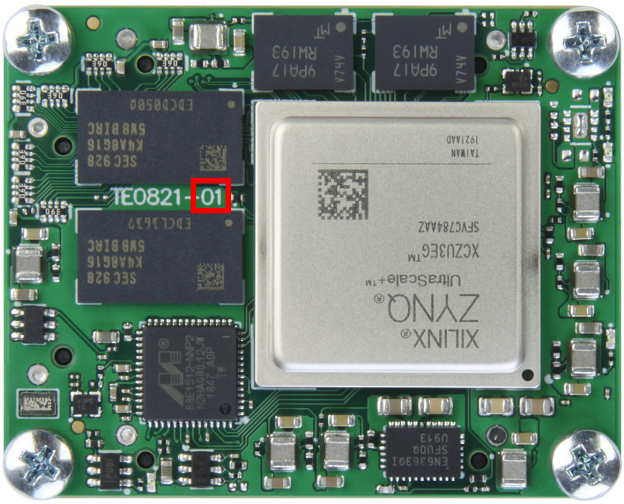
Type: Schematic change

Reason: Follow Ethernet PHY recommendation.

Impact: None.

Method of Identification

The revision number is shown on the top side of the PCB.



Production Shipment Schedule

From February 2025, after old stock is gone. If the new revision is not suitable for your application and still the former revision of the board is needed, please contact us.

Contact Information

If you have any questions related to this PCN, please contact Trenz Electronics Technical Support at

- forum.trenz-electronic.de[2]
- wiki.trenz-electronic.de[3]
- support%trenz-electronic.de[4] (subject = PCN-20240621a)
- phone
    - national calls: 05741 3200-0
    - international calls: 0049 5741 3200-0

Disclaimer

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Trenz Electronic sales office, technical support or local distributor.

This PCN follows JEDEC Standard J-STD-046.

2 http://forum.trenz-electronic.de/
3 http://wiki.trenz-electronic.de/
4 mailto:support@trenz-electronic.de?subject=PCN-20240621a